CSP Assembly Reliability Challenges

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ABSTRACT

*Availability of board **solder joint reliability** information is critical to the wider implementation of Chip Scale Packages (CSPs). This paper will compare three different CSP concepts as well as their assembly reliability A MicrotypeBGA consortium with industry-wide support was organized by the Jet Propulsion Laboratory to address technical issues regarding the interplay of package types, I/O counts, PWB (Printed Wiring Board) materials and types (standard and microvia), and manufacturing variables on quality and board reliability. The most recent results from this program will also be presented.*

Why Chip Scale Packages

Emerging Chip Scale Packages (CSPs) are competing with bare die assemblies and are now at the stage that Ball Grid Arrays (BGAs) were about two years ago. These packages provide the benefits of small size and performance of the bare die or flip chip, with the advantage of standard die packages. CSPs are defined as packages that are up to 1.2 or 1.5 times larger than the perimeter or the area of the die. Many manufacturers now refer to CSP as the package that is a miniaturized version of the previous generation. Two concepts of CSPs are shown in Figure 1. The concepts presented include: (1) packages with flex or rigid interposer and (2) wafer level molding and assembly redistribution.

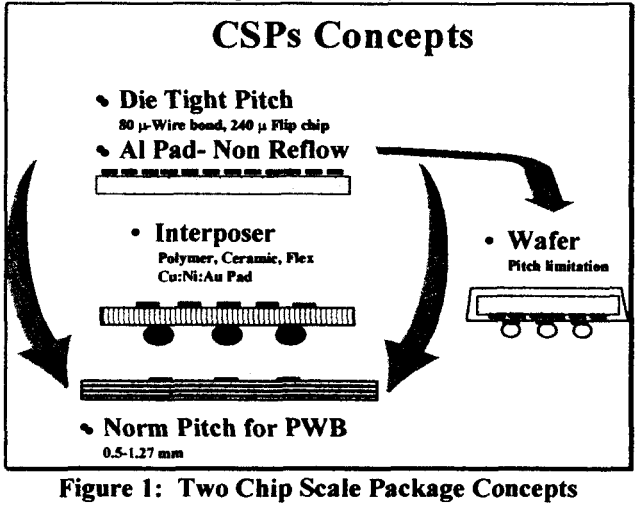


Figure 1: Two Chip Scale Package Concepts

Packaging accomplishes many purposes, including the following:

- Provides solder balls and leads that are compatible with the PWB pad metallurgy for reflow assembly processes.
- Redistributes the tight pitch of the die to the pitch level that is within the norm of PWB fabrication. The small sizes of CSPs do not permit significant redistribution and the current cost effective PWB fabrication limits full adoption of the technology, especially for high I/O counts.
- Protects the die from physical and alpha radiation damages, and provides a vehicle for thermal dissipation.
- Eases die functionality testing.

Self Alignment of Micro Type BGAs

CSPs can be categorized into grid arrays and leads (no leads) using the I/O expandability and manufacturing robustness as shown in Figure 2.

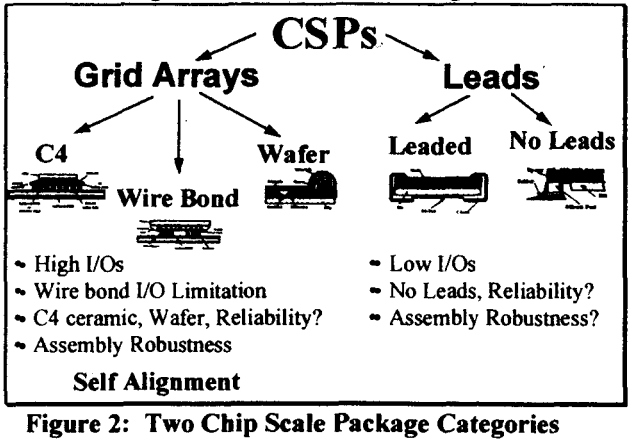


Figure 2: Two Chip Scale Package Categories

Key advantages/disadvantages of each category are also listed. The mini (fine pitch) grid arrays can accommodate higher pin counts, and similarly to BGAs, they have self alignment (centering) characteristics. For BGAs, the ease of package placement requirements has been widely published as one of their attributes. This attribute has

permitted reduction in the number of solder joint defects to lower levels than conventional SM packages.

For grid CSPs, the molten surface tensions are much smaller than BGAs since they have lower solder ball volumes. This, coupled with the CSPs finer pitch, can degrade their self alignment performance, especially with heavy packages. Therefore, the CSPs might require much tighter placement accuracy than the 50 mil pitch BGAs.

Microelectronics Assembly Reliability

A key source of damage in package attachment is caused when the system temperatures is changed. Assemblies are expected even to expose to more thermal cycles with the energy conservation trend. Previously, electronic hardware was generally left on for long periods of time which resulted in relatively few thermal cycles. Power down whenever the system is not actively used results in more cycles. This raises more concerns regarding solder joints which are affected by thermal cycling. Damages to solder joints are most often caused by the following source:

- Global CTE (Coefficient of Thermal Expansion) mismatch between the package and board induces stresses. The package and board can also have temperature gradients through the thickness and at surface areas
- Local CTE mismatch between solder attachment to component and PWB

Reducing CTE mismatch of component and PWB reduces cycling damages, but the ideal condition depends on thermal conditions of components, PWB, and solder. An ideal condition could be the CTE tailored PWB materials which have slightly higher CTE than the components. This recommendation is based on the assumption that generally the global CTE mismatch is dominant and the component with the heat generating die is hotter than the PWB.

There are other approaches to reducing damage to solder joints. Underfill application is a common technique which have been widely used for direct attachment of chip on board or when package leads are not robust. Other less conventional approaches are aimed at absorbing CTE mismatch between the die and board within the package or externally through strain absorbing mechanisms and therefore reducing stresses on the solder interconnects. These approaches could introduce their own unique damage since the weakest link now is transferred from solder to other areas of the attachment system.

CSP Assembly Reliability

Table 1 categorizes assembly reliability of packages for three levels. It includes literature reliability experiment data for packages with flex or rigid interposers and wafer level packages. Aspects of cycling conditions with their failure mechanisms are summarized in the following.

CTE Absorbed CSP

Thermal cycling test results for a CTE-mismatched relieved package are shown in the Table 1. This package uses TAB-like IC interconnects, a resilient elastomeric interposer, and eutectic solder balls. The resilient interposer in conjunction with the springiness of the TAB interconnection reduce thermal expansion differences between the chip (CTE 2-3 ppm/°C) and the PWB (CTE for FR-4 ~15 ppm/°C). This package has been shown to be reliable, robust, with no requirement for underfilling. Thermal cycling/shock data given in the Table were for daisy chain packages on FR-4 and were performed from the liquid nitrogen temperature (-196°C) to hot oil (160°C).

Because of the low strain state of solder joints, fatigue failure mechanisms of solder joints were not observed and failures shifted to the heel of TAB interconnection with high mismatched stress levels. Significant improvement was observed when ductile gold leads were used. The gold version showed no failure up to 2000 cycles in the range of -65°C to 150°C. The thermal cycling screening test results associated with assembly exposures to extremely low temperatures (stress conditions) and high temperatures (strain conditions) are not realistic and therefore their failure mechanisms may not be representative of field failures.

One such failure, due to extreme high temperature exposure, is the chambering and deformation of FR-4 close to its glass transition temperature (Tg). The PWB materials show severe damage if the cycling temperature becomes close to or exceeds their glass transition temperatures (the temperature that polymer materials start to become soft). Indeed, it was observed that FR-4 plated through holes had massive barrel cracking failure for the -65°C to 150°C temperature cycling range.

Table 1 also include the most recent results from two users. Cycles to failure are much lower than those presented by the supplier of this package. Data

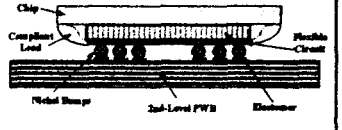
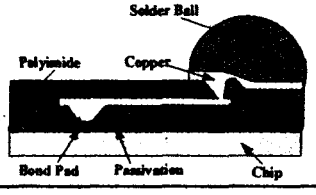
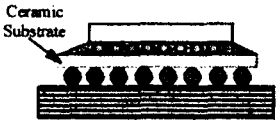
from Intel presented in late 1997 also show higher number of cycles to failure for this package than those from Motorola presented in May 1998. It is postulated that the former investigator had a more controlled package supplier whereas the latter had packages from different licensees.

Extreme CTE Mismatch

Thermal cycling test results for assembly of a wafer redistributed package is shown in Table 1. In this package, a thin film metal/polymer redistributes the location of the solder bumps over the chip to make these compatible with the surface mount footprint. The height of the package type increases by the thickness of the metal polymer layer from the bare chip. This additional layer will not generally absorb the CTE mismatch between the chip and the board and therefore the assembly reliability of these package is expected to be very similar to Controlled Collapse Chip Connection (C4) assemblies.

Without the underfill materials, the assembled package failed in less than 40 cycles when subjected to thermal cycling between 0°C and 100°C. For these types of packages, underfilling is usually required to achieve an acceptable level of assembly reliability. The underfilled assemblies did not fail up to 2,000 cycles.

Table 1 Literature Data on CSP Assembly Reliability

Package Type Schematic (not to scale)	Cycling Condition	Total Cycles	Fails/ Samples	I/O	References (comments)
Flex Interposer CTE matched 	-196°C to 160°C -65°C<>150°C -65°C to 150°C -55°C to 125°C -55°C to 125°C 5.8 cycles/hr	130 1163 750 1000 1000 no underfill 500* 600	0/3 0/46 0/78 4/78* 0/78 1/8 3/8	188 188 46 40	T. DiStefano, J. Fjelstad, "Chip-scale Packaging meets future design needs," *Solid State Technology*," April 1996 S. Greathouse," Chip Scale Package Solutions-The Pro's and Cons," Proceedings of second International Conference on Chip Scale Packaging, CHIPCON '97, Feb. 20-21, 1997 * 4/78 right after 1,000 cycles in lead Lall, P., "Assembly Level Reliability Characterization of Chip-Scale Packages," 48th Electronic Component & Technology Conference, May 25-28, 1998 * Internal TAB failure
Wafer Level Redistribution 	0°C <> 100°C (Thermal Shock)	>2000 underfill <40 no underfill	NA	266	R. Chanchani, et al, "mini Ball Gird Array (mBGA) Assembly on MCM-L Boards," *Proceedings of Electronic Components and Technology Conference*, May 18-21, 1997
Ceramic CSP 	-40°C <>125°C	~600* no underfill, PWB 0.6 mm >900* no underfill, PWB 1.6 mm	NA	220	R. Ianzone, "Ceramic CSP: A Low Cost, Adaptive Interconnect, High Density Technology," *Proceedings of second International Conference on Chip Scale Packaging, CHIPCON* '97, Feb. 20-21, 1997 *Private Communication

Ceramic Packages with Rigid Interposer

The non-wafer level ceramic packages have shown reasonable assembly reliability with no underfilling. Thermal cycling results for a ceramic package on FR-4 is also included in Table 1. The ceramic CSP uses the same design rules as multilayer ceramic (MLC) with the first level interconnection choices of thermal compression and gold stud bump, solder flip chip, and wire bond. The strength, rigidity, coplanarity, and chamber of package are excellent. The package assembly on a 0.6 mm low Tg FR-4 failed at about 600 thermal cycles between -40°C to 125°C. Cycles to failure increased to more than 900 cycles when PWB thickness increased to 1.6 mm. Thicker FR-4 is expected to show better rigidity when exposed to

125°C, a temperature close to the low Tg FR-4 polymer used for this study.

CSP Investigation

In the process of building the Consortium CSP[1] test vehicles many challenges were identified regarding various aspects of technology implementation. The overall program objectives and technology aspects are discussed below. Key challenges are summarized as follows:

Maturity and availability — Availability of CSPs for use and attachment reliability evaluation were the most challenging issues at the start of program in early 1997. There were numerous publications on a wide range of CSPs, but most packages were at their early development stage and lacked package reliability data. Assembly reliability data were even rarer. Most packages were only available in prototype forms, and this, of course, did not guarantee the package similarity to the production version or even their future availability. More than six month delay on package delivery date was the norm. Four packages dropped out of the program, and one was delayed almost a year. Although many suppliers promoted their packages and package reliability, they were not willing to submit their packages for an independent evaluation, possibly because of lack of confidence.

Lack of Design Guideline Standards—Guidelines and standards on various elements of CSPs were not available. For our design, guidelines developed by the package suppliers were used when available. Otherwise, available knowledge and engineering judgment were utilized.

PWB Build — The standard PWB design could be used for low I/O CSPs. Build up (microvia) board technology is required for higher I/O CSPs in real application with active die. For daisy chain packages, it is possible to design high I/O on a standard board. Board design guidelines are needed, especially for the build up (microvia) configuration.

Applications — There were a number of packages from low I/O (<50) to higher I/Os (about 500) for characterization. It became apparent that for the near future, 1-3 years, the dominant packages would be those with less than 50 I/Os. Specific application requirements could utilize packages with much higher I/Os. Mixture of conventional SM (surface mount) packages, direct chip attachment (DCA), BGAs, and CSPs on one board is another expected design and assembly challenge. This mixed technology is being considered for the next test vehicle under the second JPL-led CSP Consortium.

ASSEMBLY

The Consortium assembled seven trial #1 test vehicles and 30 #2 test vehicles. Ball grid arrays are known to be robust in manufacturing, but there is disagreement on the acceptable manufacturing offsets for CSPs. No defects were observed when thirty #2 test vehicles, each with 4 grid CSPs with 46 I/Os, were assembled.

THERMAL CYCLING TEST RESULTS

Seven trial #1 test vehicles were assembled to optimize the assembly process and profile. The lowest stencil thickness, 4 mil, was used to determine the worst condition, that is, solder starving condition on a leadless package. A stencil thickness of 6 mil is the recommended thickness for assembly of leadless packages. One test vehicle was assembled double sided. Five of the PWBs had OSP surface finish, and two had HASL. All PWBs including the PWBs with HASL finish, were successfully assembled. As expected, working with HASL was much more difficult than OSP.

The five trial test vehicles with the OSP finish were subjected to thermal cycling in the range of -30 to 100°C (A condition). Both PWB and assembly conditions were not optimum for the trial test. Therefore, thermal cycling results may well suggest potential areas where the process can be optimized for the production test vehicle assemblies. Results are not valid for reliability and failure statistic analyses because of low number of test samples and no-optimum condition.

Resistances were measured manually before and at different thermal cycling intervals to check for electrical opens (solder joint failure). Automatic monitoring was impossible since connections to the ground plane were missed during file translation. This has been corrected and for full production assemblies, these daisy chains will be monitored continuously.

Table 2 shows resistances before and at different thermal cycles. Assemblies were periodically removed from the chamber and checked at room temperature for resistance (Ω). Resistance are different for different daisy chain patterns, but are approximately the same for the same package on various test vehicle assemblies. It is interesting to note that even for non-optimum conditions, the majority of solder joint assemblies survived to 500

cycles. These packages included four low I/O CSPs, leadless and grid CSPs, one high I/O CSP, and a TSOP. The high I/O CSP was underfilled.

The test vehicle with identification 21-1 and 21-A was the board with the double sided packages. The microvia side (21-A) was reflowed first, and the standard side (21-1) was reflowed next. Therefore, the microvia joints were exposed to two reflows, but the standard side only once. One failure of a leadless package was observed between 100 and 300 cycles (21-A, daisy chain 1) on the microvia side. This package was also the only package which exactly overlapped the package on the double side with 90 degree rotation.

Table 2 Daisy Chain Resistances of Assembled CSPs at Various Number of Cycles at Condition A (-30/100°C)

PWB ID	Package ID-Daisy	Cycle 0	Cycle 100	Cycle 300	Cycle 400	Cycle 500	Cycle 600
22-1A	1	2.8	2.8	Open	Open	Open	Open
22-1A	2	4.6	4.7	5.4	4.8	4.8	4.8
22-1A	3	9.3	9.2	9.5	9.3	9.4	9.5
22-1A	4	6.8	6.6	7	6.8	6.8	6.6
22-1A	5	5.8	5.7	6	6.2	5.7	5.9
22-1A	6-1	20.9	20.7	21.2	21.1	21.2	21.1
22-1A	6-2	23.7	23.5	23.8	23.7	23.6	23.7
22-1	1	2.3	2.3	2.6	2.7	2.6	2.4
22-1	2	4	4.1	4.1	4.3	4.2	4.1
22-1	3	9.3	9.3	9.4	9.4	9.2	9.2
22-1	4	5.9	6.3	5.9	6.2	5.8	5.8
22-1	5	6.1	6.2	6.9	6.6	6.9	6.3
22-1	6-1	Open	Open	Open	Open	Open	Open
22-1	6-2	28.6	Open	Open	Open	Open	Open
29-1	1	2.8	2.8	2.9	3	2.9	2.8
29-1	2	4.6	4.8	5.1	4.9	4.9	4.8
29-1	3	9.7	9.6	9.6	9.7	9.7	9.6
29-1	4	6.7	6.8	7	7	6.8	7
29-1	5	5.6	5.7	5.7	5.6	5.7	5.7
29-1	6-1	21.6	21.6	21.7	21.8	21	21.6
29-1	6-2	24.5	24.6	24.6	24.7	23.5	24.8
3-1	1	2.8	2.8	2.9	2.9	2.9	2.6
3-1	2	4.7	4.7	4.9	5.1	4.8	4.7
3-1	3	9.5	9.4	9.6	9.7	9.6	9.8
3-1	4	6.8	6.7	7	7	7.1	6.9
3-1	5	5.7	5.6	6	5.9	5.9	5.6
3-1	6-1	19.2	19.1	19.4	19.2	19.8	19.1
3-1	6-2	22.8	22.6	22.9	22.9	22.7	22.6
19-1	1	2.8	2.7	2.9	3.2	2.9	STOP
19-1	2	4.8	4.7	5	4.6	4.7	STOP
19-1	3	10	10	10.1	10.3	10.6	STOP
19-1	4	6.8	6.8	6.9	6.7	6.5	STOP
19-1	5	7.8	Open	Open	Open	Open	STOP
19-1	6-1	23.3	23.3	23.3	23.7	24.7	STOP
19-1	6-2	24.8	24.7	24.8	25	23.3	STOP

The first failure location was at a two cross-over corners. The criticality of solder disturbance at the crossing corners will be verified in the full production test vehicle build. Early joint failure is qualitatively in agreement with other investigators' findings. The number of cycles-to-failure was reduced to almost half for double sided assemblies with the mirrored package assemblies. The number of cycles-to-failure was increased as double sided package assemblies moved away from the mirror position.

The other failures of 21-1, daisy chain 6-1 and 6-2, and 19-1, daisy chain 5, were considered to be defects related either to the package or the PWB or both. One was due to the use of preproduction package (not the same as the one to be used for full production), and the other due to package and process anomalies. Via misregistration and solder mask coverage on the pads could have been the potential cause of joint failure on the PWB. Recall that these test vehicles were from the trial run, the chief purpose of which was to understand the critical issues with of PWB fabrication, process optimization, and daisy chain verification.

Table 3 Number Solder Joint Failures for Low I/O Wafer Level Assemblies before and up to 500 Thermal Cycles (-30 to 100 °C)

Package	Total of TV	U1 Site	U2 Site
As Assembled	31	0	3
0 Cycles	10	0	1
100 Cycles	10	0	2
200 Cycles	10	0	2
300 Cycles	10	0	2+ 1 Resistance 13.1Ω
400 Cycles	10	0	2+ 1 Resistance 13.7Ω
500 Cycles	10	0	2+ 1 Resistance 16.4Ω

CSP TECHNOLOGY RANKING METRICS

Currently, there are nearly 50 commercially available CSPs within different categories. Each type has its strong features and characteristics. The CSPs' attributes cannot easily be quantified since they are influenced by many factors, including supplier approach and user requirements. A qualitatively comparison of different technologies is possible. Table 4 shows such a comparison. As a benchmark, it include the flip chip technology.

CSPs were ranked for their features, including cost, yield, availability, reliability, and testability. The highest ranking is for CSPs with a flex interposer and the lowest for wafer distribution. CSPs with leads/no leads were ranked the same as the rigid interposer packages. Reworkability and reliability of leads/no lead with a very low I/O was considered to be better, whereas CSPs with rigid interposers better accommodate the higher I/O requirement.

CONCLUSIONS

- Mixed technology assembly may not easily permit the use of optimum solder volume to achieve the highest reliability. This is probably true for an SM mixture of fine pitch and leadless packages and become challenging with the addition of no-lead (leadless) and grid CSPs. CSPs, reliability may be degraded in a mixed technology assembly, especially for no-lead CSPs.
- Low lead small wafer level CSP packages exhibited poor quality. Three out of 62 failed after assembly and another failed after 100 condition A cycles.
- The trial test vehicles assembled for process optimization (non-optimum condition) were subjected to cycling (A condition). The solder joints on double sided assembly were the first to fail among many leadless and grid CSPs. This agree with other investigators' test results which shown deleterious effects of double sided assemblies on solder joint reliability.
- Traditionally, solder joint failure was considered to be the weakest link in the microelectronics attachment reliability. This might not be true for CSPs with an innovative design.
- Cycling temperature range in some cases might be severe and introduce failure mechanisms that are not representative of field applications. Complimentary tests and failure analyses need to be performed to build confidence in assembly reliability results.
- Understanding the overall philosophy of testing to meet system requirements as well as detecting new failure mechanisms associated with the miniaturized CSPs is the key to collecting meaningful test results.

Table 4 Different CSP Technology Rankings Compared to Flip Chip

Package Types-> Merits	Wafer	Lead/ No Lead	Interposer Flex	Interposer Rigid	Wafer Redist	Flip Chip
Cost Device	3	3	9	9	3	3
Cost PWB/PWA	9	9	9	9	1	1
Yield	9	9	9	9	3	1
Compatability	9	9	9	9	3	1
Availability/Multiple Sources	1	9	9	9	3	1
Flexibility	1	3	9	9	3	3
Testability	9	9	9	9	3	3
Reworkability	3	9	9	3	1	1
Reliability	3	9	9	3	1	1
I/O	4<>64	10<>64	10<>400		100<>2000	100<>2000
	47	**69**	**81**	**69**	**21**	**15**

9 = Good, 3 = Fair, 1 = Poor

REFERENCES

[1] Ghaffarian, R., et al "CSP Consortia Activities: Program Objectives and Status," Proceedings of Surface Mount International, San Jose, CA, Sept 23-27, page 507, 1998

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